CLAIMS

We claim:

1. An electronic package for a device, comprising:

an interconnect substrate having an upper surface and a lower surface;

a die attach pad on said upper surface for receiving a semiconductor device chip;

a heat spreader on said lower surface, said heat spreader positioned beneath said die attach pad;

a plurality of vias passing through the thickness of said interconnect substrate from said upper surface to said lower surface;

a first group of said vias positioned to intersect both said die attach pad and said heat spreader;

a second group of said vias positioned about and spaced away from said die attach pad;

a thermal conductor located in said first group to thermally interconnect said die attach pad and said heat spreader;

a plurality of bond pads positioned on said upper surface, each of said plurality of bond pads abutting one of said vias of said second group;

a plurality of lands positioned on said lower surface, each of said plurality of lands abutting one of said vias of said first group; and

an electrically conductive medium located in said second group to electrically interconnect each of said plurality of bond pads to said plurality of lands.

2. The electronic package of claim 1, wherein said interconnect substrate is constructed from an organic material.

3. The electronic package of claim 1, wherein said interconnect substrate is constructed from a ceramic material.

4. The electronic package of claim 1, wherein said plurality of bond pads are positioned in a peripheral design.

5. The electronic package of claim 1, wherein said plurality of bond pads are positioned in an array of columns and rows.

6. The electronic package of claim 1, wherein at least one of said plurality of bond pads is co-located with one of said vias of said second group.

7. The electronic package of claim 1, wherein at least one of said plurality of lands is co-located with one of said vias of said second group.

8. A semiconductor device comprising:

an interconnect substrate having an upper surface and a lower surface;

a die attach pad on said upper surface;

a heat spreader on said lower surface, said heat spreader positioned beneath said die attach pad;

a plurality of vias passing through the thickness of said interconnect substrate from said upper surface to said lower surface;

a first group of said vias positioned to intersect both said die attach pad and said heat spreader;

a second group of said vias positioned about and spaced away from said die attach pad;

a thermal conductor located in said first group to thermally interconnect said die attach pad and said heat spreader;

a plurality of bond pads positioned on said upper surface, each of said plurality of bond pads abutting one of said vias of said second group;

a plurality of lands positioned on said lower surface, each of said plurality of lands abutting one of said vias of said second group;

an electrically conductive medium located in said second group of vias to electrically interconnect each of said plurality of bond pads to said plurality of lands; and

a semiconductor device chip attached to said die attach pad and having a plurality of device electrodes on a surface thereof.

9. The semiconductor device of claim 8 further comprising electrical bonds connecting said plurality of device electrodes to said plurality of bond pads.

10. The semiconductor device of claim 8, wherein said interconnect substrate is constructed from an organic material.

11. The semiconductor device of claim 8, wherein said interconnect substrate is constructed from a ceramic material.

12. The semiconductor device of claim 8, wherein said plurality of bond pads are positioned in a peripheral design.

13. The semiconductor device of claim 8, wherein said plurality of bond pads are positioned in an array of columns and rows.

14. The semiconductor device of claim 8, wherein at least one of said plurality of bond pads is co-located with one of said vias of said second group.

15. The semiconductor device of claim 8, wherein at least one of said plurality of lands is co-located with one of said vias of said second group.

16. The semiconductor device of claim 8, wherein said electrical bonds comprise wires.

17. The semiconductor device of claim 8, further comprising an electrical connection from a surface of said semiconductor device chip to said die attach pad.

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